Digital Logic Design Using Verilog: Coding and RTL Synthesis

By Vaibbhav Taraate

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This book is designed to serve as a hands-on professional reference with additional utility as a textbook for upper undergraduate and some graduate courses in digital logic design. This book is organized in such a way that that it can describe a number of RTL design scenarios, from simple to complex. The book constructs the logic design story from the fundamentals of logic design to advanced RTL design concepts. Keeping in view the importance of miniaturization today, the book gives practical information on the issues with ASIC RTL design and how to overcome these concerns. It clearly explains how to write an efficient RTL code and how to improve design performance. The book also describes advanced RTL design concepts such as low-power design, multiple clock-domain design, and SOC-based design. The practical orientation of the book makes it ideal for training programs for practicing design engineers and for short-term vocational programs. The contents of the book will also make it a useful read for students and hobbyists.

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Editorial Review

Review
"This book presents digital logic design using the hardware description language known as Verilog. … The book will help readers learn digital logic design and become familiar enough with it to work with it further in the future. It is mainly aimed as a textbook for undergraduate students to implement digital logic design in a lab. The book discusses logic design in a well-structured way covering basic to intermediate concepts." (J. Arul, Computing Reviews, April, 2017)

From the Back Cover
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About the Author
Vaibbhav Taraate is Entrepreneur and Mentor at "Semiconductor Training @ Rs.1". He holds a BE (Electronics) degree from Shivaji University, Kohlapur in 1995 and secured a gold medal for standing first in all engineering branches. He has completed his MTech (Aerospace Control and Guidance) in 1999 from IIT Bombay. He has over 15 Years of experience in semi-custom ASIC and FPGA design, primarily using HDL languages such as Verilog and VHDL. He has worked with few multinational corporations as consultant, senior design engineer, and technical manager. His areas of expertise include RTL design using VHDL, RTL design using Verilog, complex FPGA-based design, low power design, synthesis/optimization, static timing analysis, system design using microprocessors, high speed VLSI designs, and architecture design of complex SOCs.

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